100Gb/S QSFP28 eSR4 Transceiver(Extended Reach)

P/N: TQSFP28-EJ1P85C

Product Features

- Compliant with 100G Ethernet IEEE 802.3bm 100GBASE-SR4 standards
- SFF-8665 Revision 1.8 Compliant
- Supports 100 Gbps data rate links of 300m via OM4
- Low power consumption of max 2.5W (Typ. 1.8W)
- Hot pluggable electrical interface
- 0 to 70°C case temperature operating range
- RoHS-6 Compliant

Application

- 100GBASE-SR4 Ethernet links
- InfiniBand EDR, FDR, & QDR
- HPC Interconnects
- Proprietary Interconnections

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Absolute Maximum Rating

Parameter	Min	Max	Unit	Note
Storage Temperature	-40	85	℃	
3.3V Power Supply Voltage	-0.5	3.6	V	
Data Input Voltage- Single Ended	-0.5	Vcc+0.5		
Control Input Voltage	-0.5	3.6	V	1
Relative Humidity	5	85	%	
Rx Optical Damage Threshold / Lane	3.4		dBm	

Notes:

1. Non-condensing

Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Note
Case Operating Temperature	0	40	70	℃	
Power Supply Voltage	3.135	3.3	3.465	V	
Date Rate per Channel		25.78125		Gbps	
Bit Error Ratio		10^{-12}			
Control Input Voltage High	2		Vcc+0.3	V	
Control Input Voltage Low	-0.3		0.8	V	
Two Wire Serial (TWS) Interface Clock Rate		100	400	kHz	
Differential Data Input / Output Load		100		Ohms	
Fiber Length: 4700 MHz·km 50/125μm MMF (OM4)			300	m	

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Electrical Characteristics

Parameter	Min	Typical	Max	Unit	Note
Transceiver Electrical Characteristics					
TRx Power Consumption		1.8	2.5	W	
TRx Power-on Initialization Time			2000	ms	
CAUI-4 Module Electrical Input Characteristics (TP1)					
Signaling Rate per Lane		25.78125		Gbps	1
Differential pk-pk input voltage tolerance			900	mV	
Differential Input Return Loss		See Eq. 1			2
Differential to Common-mode Input Return Loss		See Eq. 2			3
Differential termination mismatch			10	%	
Module stressed input test		See Eq. 3			4
Single Ended Input Voltage Tolerance	-0.4		3.3	V	
DC common mode voltage	-350		2850	mV	

Notes:

1. Signaling rate tolerance is within +/- 100ppm.
2. $$RLd(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}\left(\frac{f}{14}\right) & 8 \leq f < 19 \end{cases} \text{ (dB)} \qquad \text{(Eq.1)}$$

   Where

   f is the frequency in GHz

   RLd is the CAUI-4 Chip-to-module input differential return loss

3. $$RLdc(f) \geq \begin{cases} 22 - 20\left(\frac{f}{25.78}\right) & 0.01 \leq f < 12.89 \\ 15 - 6\left(\frac{f}{25.78}\right) & 12.89 \leq f < 19 \end{cases} \text{ (dB)} \qquad \text{(Eq.2)}$$

   where

   f is the frequency in GHz

   RLdc is the CAUI-4 Chip-to-module input differential to common mode input return loss

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4. The module stressed input tolerance is measured using the procedure defined in 83E.3.4.1.1, IEEE802.3bm. Module stressed input parameters include.
   a. Eye width of 0.46 UI.
   b. Applied pk-pk sinusoidal jitter is per Table 88-13 per IEEE802.3bm
   c. Eye height of 95mV

Parameter	Min	Typical	Max	Unit	Note
CAUI-4 Module Electrical Output Characteristics (TP4)					
Signaling Rate per Lane		25.78125		Gbps	1
AC Common-Mode Output Voltage (RMS)			17.5	mV	
Differential Output Voltage			900	mV	
Eye Width	0.57			UI	
Eye Height, Differential	228			mV	
Vertical Eye Closure			5.5	dB	
Differential Output Return Loss	See Eq. 1				2
Common to Differential Mode Conversion Return Loss	See Eq. 2				3
Differential termination mismatch			10	%	
Transition Time (20% to 80%)	12			ps	
DC Common Voltage	-350		2850	mV	

Notes:

1. Signaling rate tolerance is within +/- 100ppm.
2. $$RLd(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}\left(\frac{f}{14}\right) & 8 \leq f < 19 \end{cases} \text{ (dB)} \qquad \text{(Eq.1)}$$

   where

   f is the frequency in GHz

   RLd is the CAUI-4 Chip-to-module host output differential return loss

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3. $RLdc(f) \geq \begin{cases} 22 - 20\left(\frac{f}{25.78}\right) & 0.01 \leq f < 12.89 \\ 15 - 6\left(\frac{f}{25.78}\right) & 12.89 \leq f < 19 \end{cases}$ (dB) (Eq.2)

where

f is the frequency in GHz

RLdc is the CAUI-4 Chip-to-module output common to differential mode conversion return loss

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Transmitter Optical Characteristics						
Center Wavelength	λ	840		860	nm	
Spectral Width – RMS	Δλ		0.55		nm	
Average Launch Optical Power, each lane	LOP	-8.4		4	dBm	
Optical Modulation Amplitude, each lane	OMA	-6.4		4	dBm	
Launch power in OMA minus TDEC		-7.3			dBm	1
Transmitter and dispersion eye closure (TDEC), each lane	TDEC			4.3	dB	1
Average launch power of OFF transmitter, each lane				-30	dBm	
Extinction Ratio	ER	2			dB	
Optical return loss tolerance				12	dB	
Encircled Flux		≥ 86% @ 19um, ≤ 30% at 4.5um				1
Transmitter eye mask definition		(X1, X2, X3, Y1, Y2, Y3) = (0.3, 0.38, 0.45, 0.35, 0.41, 0.5)				2

Notes:

1. Designed target and belonging to TDP for further confirmation.
2. Hit ratio 1.5 × 10–3 hits per sample.
3. Y3 of mask definition is set to 0.5 per IEEE802.3bm 100G-SR4, which is subject to change to allow a specially reshaped eye for 300m linkage.

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Parameter	Symbol	Min	Typical	Max	Unit	Note
Receiver Optical Characteristics						
Center wavelength, each lane	λ	840		860	nm	
Damage Threshold		3.4			dBm	
Average power at receiver input, each lane		-10.3		2.4	dBm	1
Receiver Power, each lane (OMA)				3	dBm	
Receiver Reflectance				-12	dB	
Stressed receiver sensitivity in OMA				-5.2	dBm	
Conditions of stressed receiver sensitivity test:						
Stressed eye closure (SEC)			4.3		dB	2
Stressed eye J2 Jitter			0.39		UI	2
Stressed eye J4 Jitter,				0.53	UI	2
OMA of each aggressor lane				3	dBm	2
Stressed receiver eye mask definition		(X1, X2, X3, Y1, Y2, Y3) = (0.28, 0.5, 0.5, 0.33, 0.33, 0.4}				3

Notes:

1. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. TDP value and dependent parameters are subject to confirmation.
3. Hit ratio 5×10^{-5} hits per sample

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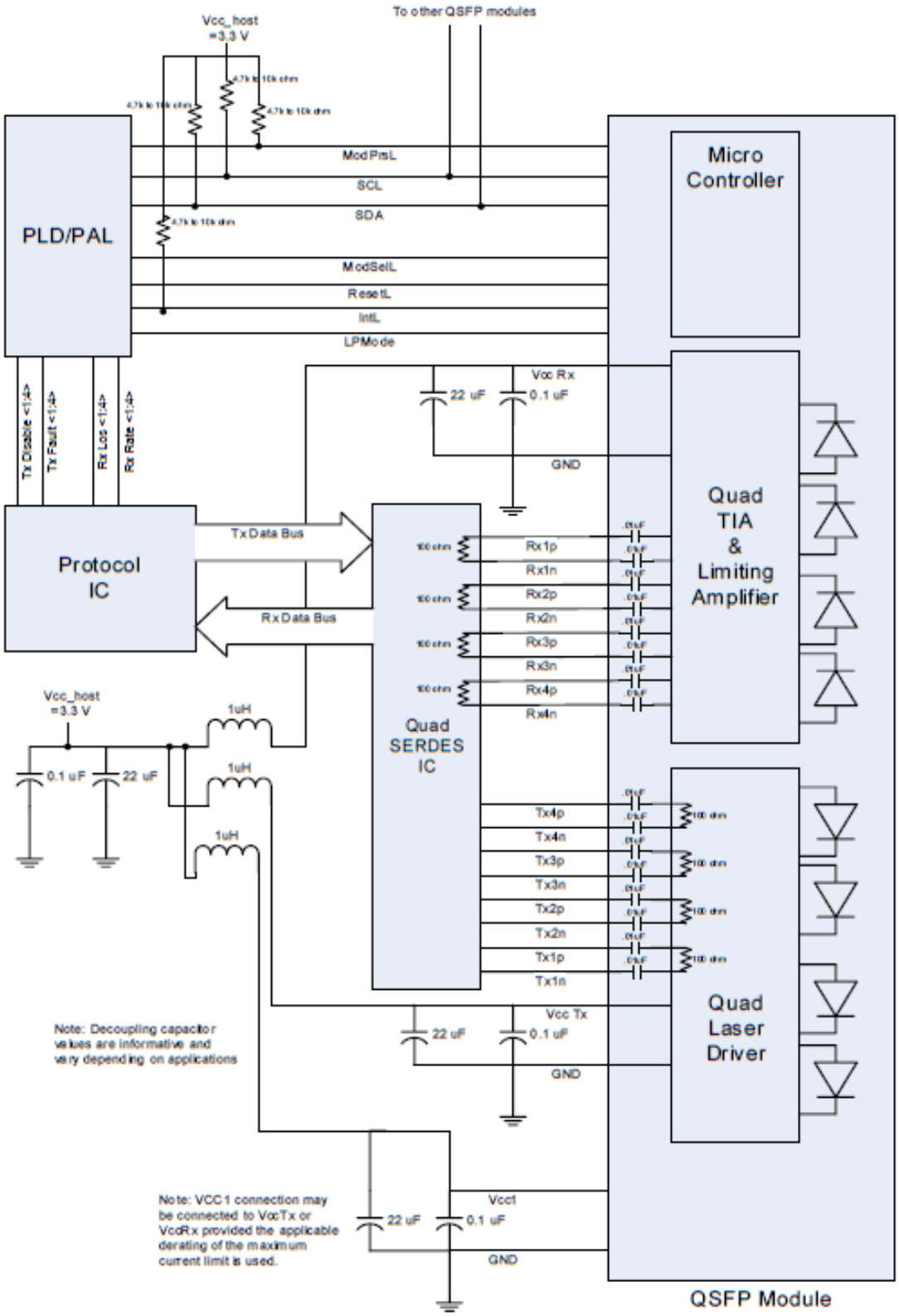
Recommended Interface Circuit



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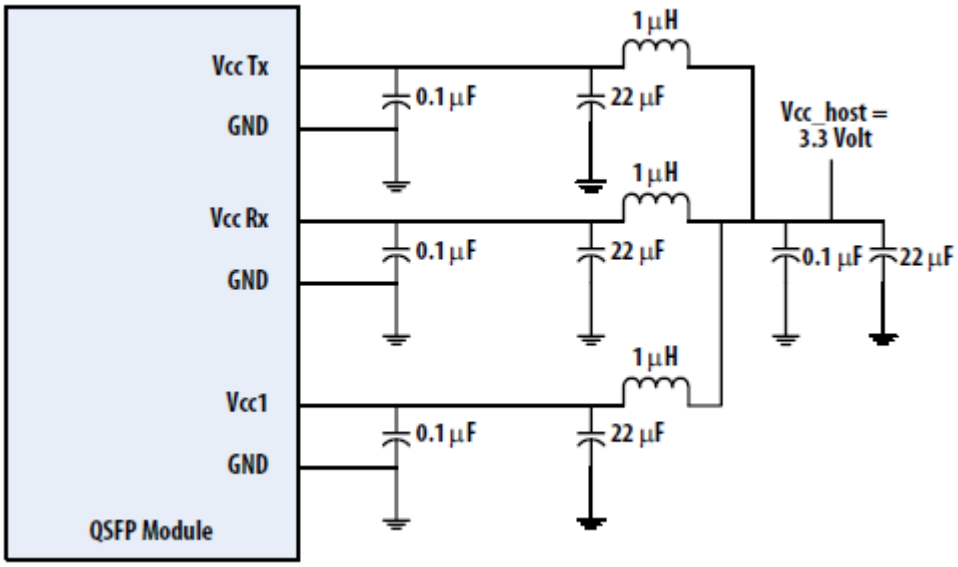
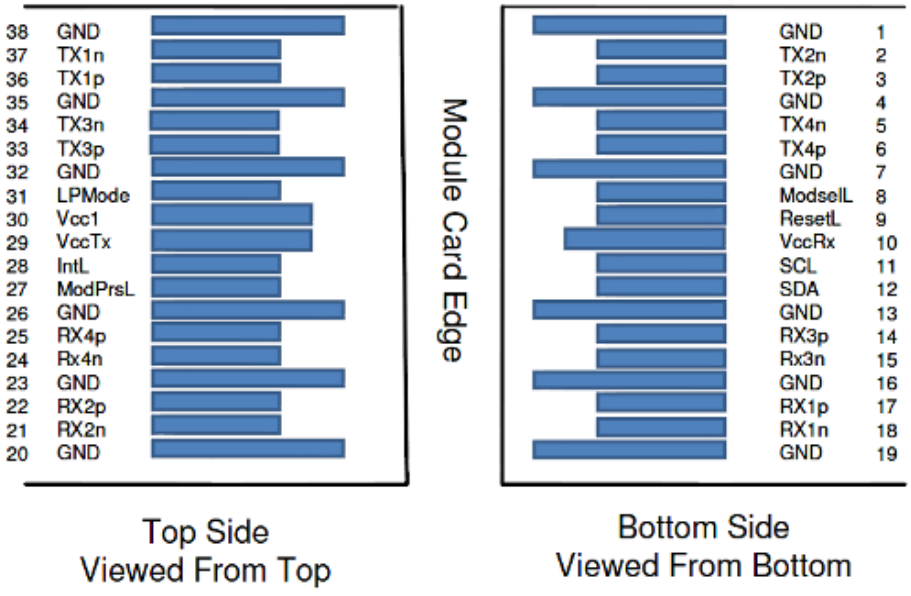
Recommended Host Board Power Supply Circuit



QSFP28 Module Pad Assignments and Descriptions



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Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	
20		GND	Ground	1	
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	
30		Vcc1	+3.3V Power supply	2	
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	

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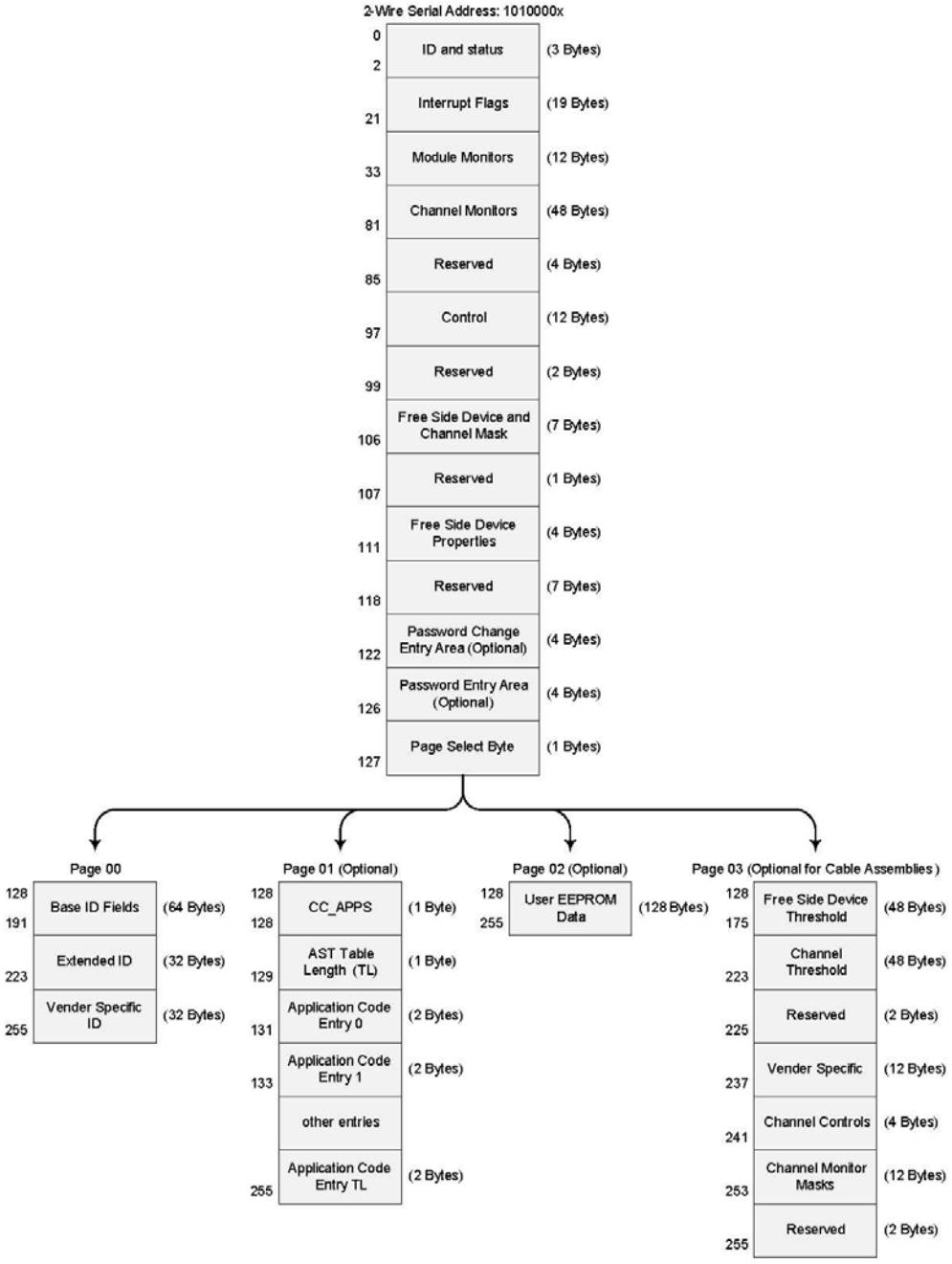
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	

Memory Map



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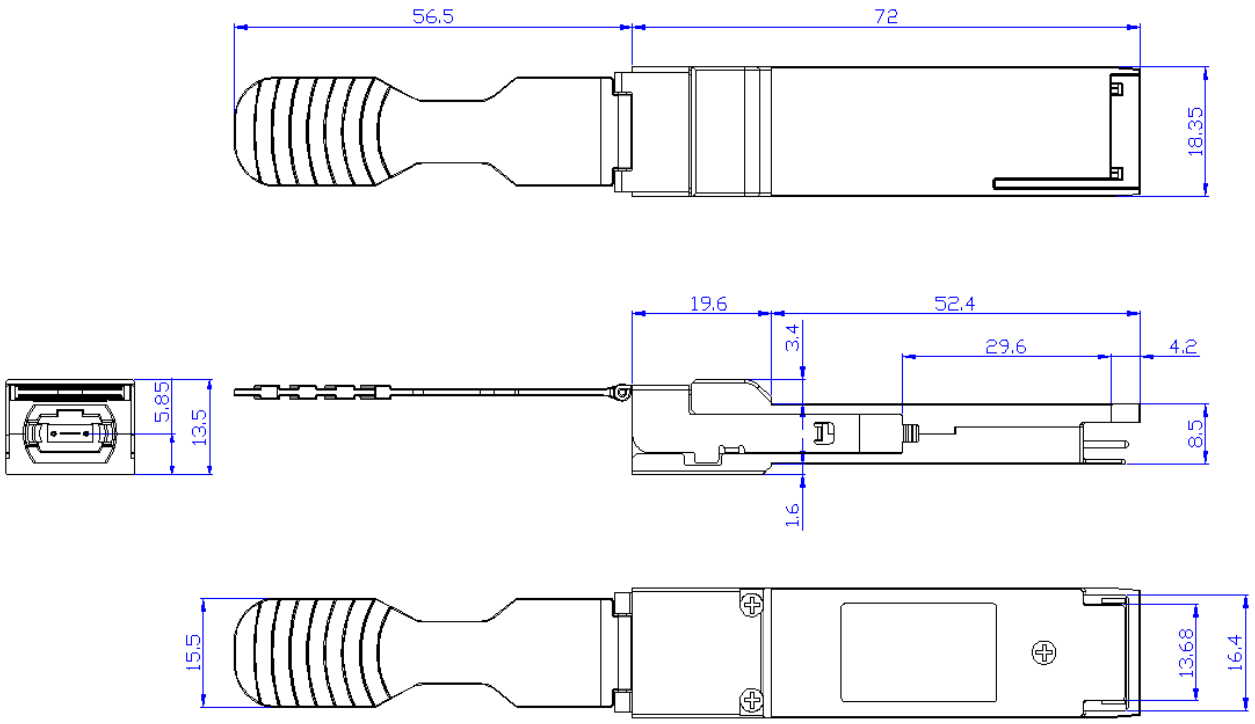
Mechanical Design Diagram

Unit: mm



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