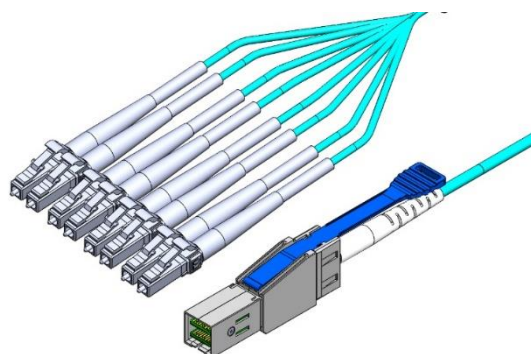


## **48Gb/S Mini-SAS HD Break-Out to 4 × LC Duplex**

**P/N: ACA-MAXCA1**



### **Product Features**

- Compliant to SFF-8644 MSA standard in mechanical consideration
- Management interface compliant to SFF-8636
- 4Tx/Rx, Full-Duplex AOCs, Maximum aggregate speed of 48-Gbps for SAS3.0
- Backwards compatible to 6-Gbps SAS-2.1 of optical-mode capable systems with out-of-band (OOB) signal supported
- Bit-Error-Rate (BER) better than  $10^{-12}$
- Round cable with small 3.0-mm outer diameter for flexible routing and easy cable management

## Absolute Maximum Rating

Parameter	Min	Max	Unit	Note
Storage Temperature	-10	70	°C	1
3.3V Power Supply Voltage	-0.5	3.6	V	
Data Input Voltage- Single Ended	-0.5		V <sub>cc</sub> +0.5	
Relative Humidity	5	85	%	2

### Note:

1. Limited by the fiber cable jacket, not the active ends.
2. Non-condensing.

## Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Note
Case Operating Temperature	0	40	70	°C	
Power Supply Voltage	3.135	3.3	3.465	V	
Data Rate per Channel		12		Gbps	
Power Supply Noise Ripple Susceptibility (PSNR)			50	mV	1
Bit Error Ratio		10 <sup>-12</sup>			2
Control Input Voltage High	2		V <sub>cc</sub> +0.3	V	
Control Input Voltage Low	-0.3		0.8	V	
Two Wire Serial (TWS) Interface Clock Rate		100		kHz	
Differential Data Input / Output Load		100		Ohms	
Standard Cable Lengths		30		m	
Electrical Connector	Four-layers 36-pins			SFF-8644	
Management Interface	Two-Wire Serial			SFF-8636	

### Notes:

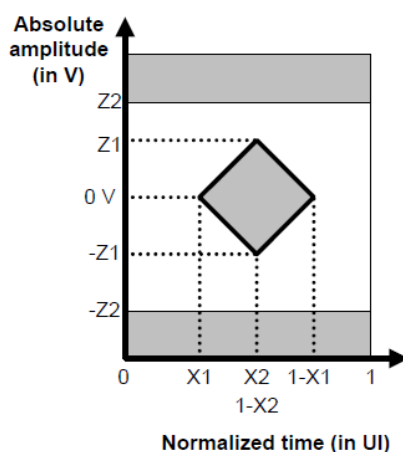
1. Power supply noise is defined as peak-to-peak noise amplitude over 1K to 15 MHz frequency range at host supply side by the recommended power supply filter for module. See Section 10 for the recommended power supply filter.
2. Bit-Error-Rate test can be compliant to SCRAMBLED\_0 defined in Working Draft SAS Protocol Layer - 3 (SPL-3). For this customized product, two identical Mini-SAS HD modules for two ends are required to ensure the 10<sup>-12</sup> BER performance.

## Electrical Characteristics

Parameter	Min	Typical	Max	Unit	Note
<b>Transceiver</b>					
TRx Power Consumption			1	W	
Transceiver Power-on Initialization Time			2000	ms	1
<b>Transmitter</b>					
Maximum input peak to peak voltage (2× Z2)			1200	mVpp	2
Minimum input eye opening (2× Z1)	200			mVpp	2
Maximum half of TJ (X1)			0.175	UI	2
Maximum RJ			0.15	UI	2
Center of bit time (X2)		0.5		UI	2
<b>Receiver (each Lane)</b>					
Maximum output peak to peak voltage (2× Z2)			1200	mVpp	2
Minimum out eye opening (2× Z1)	360			mVpp	2
Maximum half of TJ (X1)			0.35	UI	2
Maximum RJ			0.45	UI	2
Center of bit time (X2)		0.5		UI	2

### Notes:

1. "Initialization Time" is the time from when the supply voltages reach and remain above the minimum "Recommended Operating Conditions" to the time when the module enables TWS access. The module at that point is fully functional.
2. Refer to the 12Gbps active cable eye mask from SAS-3 working draft Rev. 06 (Nov. 7, 2013) of Figure 102 and Table31.



## Optical Cable Specification

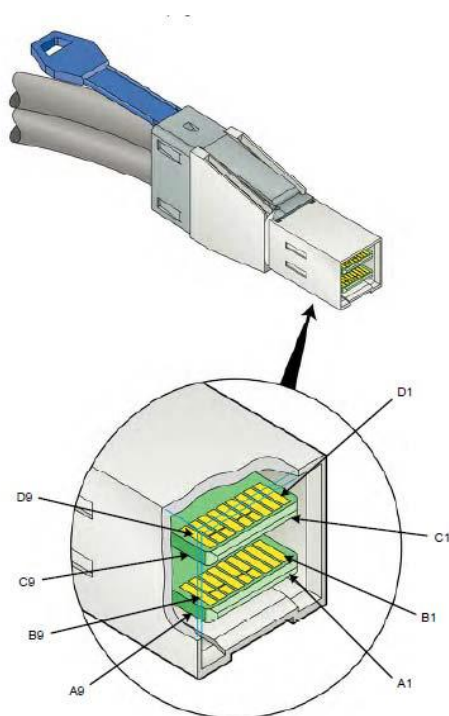
Parameter	Specification	Notes
Minimum Cable Bending Radius	30 mm	
Cable Cross-Section Dimension	Round Type Cable with 3 mm in Dia.	
Cable Cover Type	LSZH or Customization	1
Standard Cable Length	5-m (4m+1m)	2
Cable Length Tolerance	+0.5 / -0 m	

### Notes:

1. Cable cover type standard is LSZH. Other types can be available upon request.
2. Different cable length may be recommended to adopt different multi-mode fiber (MMF) grades of OM2, OM3, or OM4.

## Connector Pad Assignments and Descriptions

The Mini-SAS HD AOC plug connector is the 4 lane cable (free) connector defined in SFF-8644. The figure shows the appearance Mini-SAS HD cable plug connector.



Signal	Pin	Mating Level	Definition
Reserved	A1	Second	Reserved for future use
IntL	A2	Second	Management interface interrupt signal
GND	A3	First	Signal ground
RX1+	A4	Third	Fixed side receiver channel 1 non-inverting input
RX1-	A5	Third	Fixed side receiver channel 1 inverting input
GND	A6	First	Signal ground
RX3+	A7	Third	Fixed side receiver channel 3 non-inverting input
RX3-	A8	Third	Fixed side receiver channel 3 inverting input
GND	A9	First	Signal ground
Vact	B1	Second	Free side power input for non-management interface circuitry
ModPrsL	B2	Second	Free side active low present output
GND	B3	First	Signal ground
RX0+	B4	Third	Fixed side receiver channel 0 non-inverting input
RX0-	B5	Third	Fixed side receiver channel 0 inverting input
GND	B6	First	Signal ground
RX2+	B7	Third	Fixed side receiver channel 2 non-inverting input
RX2-	B8	Third	Fixed side receiver channel 2 inverting input
GND	B9	First	Signal ground
SCL	C1	Second	Management interface serial clock
SDA	C2	Second	Management interface serial data output
GND	C3	First	Signal ground
TX1+	C4	Third	Fixed side transmitter channel 1 non-inverting output
TX1-	C5	Third	Fixed side transmitter channel 1 inverting output
GND	C6	First	Signal ground
TX3+	C7	Third	Fixed side transmitter channel 3 non-inverting output
TX3-	C8	Third	Fixed side transmitter channel 3 inverting output
GND	C9	First	Signal ground
Vact	D1	Second	Free side power input for non-management interface circuitry
Vman	D2	Second	Free side power input for management interface circuitry
GND	D3	First	Signal ground
TX0+	D4	Third	Fixed side transmitter channel 0 non-inverting output
TX0-	D5	Third	Fixed side transmitter channel 0 inverting output
GND	D6	First	Signal ground
TX2+	D7	Third	Fixed side transmitter channel 2 non-inverting output
TX2-	D8	Third	Fixed side transmitter channel 2 inverting output
GND	D9	First	Signal ground

## Mechanical Design Diagram

Unit: mm

