40Gb/S QSFP+ LR4 Transceiver

P/N: TQSFPP-CC1FAAD

Product Features

- Compliant with IEEE 802.3ba 40G BASE-LR4 standards
- QSFP+ MSA compliant
- Maximum power consumption 2.5W
- 4 CWDM lanes MUX/DEMUX design
- Single 3.3V power supply
- 0°C to 70°C case temperature operating range
- LC duplex connector
- Maximum link length of 10km on SMF
- I2C management interface
- RoHS-6 Compliant

Application

- Ethernet for 40GBASE-LR4
- InfiniBand SDR, DDR and QDR
- High-speed Servers
- High-performance Computing Clusters
- SAN, Routers, Hubs, Load Balancer

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Absolute Maximum Rating

Parameter	Min	Max	Unit	Note
Storage Temperature	0	85	℃	
Relative Humidity	0	85	%	

Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Note
Case Operating Temperature	0	40	70	℃	
Power Supply Voltage	3.15	3.3	3.45	V	
Data Rate per Channel		10.3125		Gbps	
Power Supply Noise			50	mVpp	
Supply Noise Rejection			100	mV	
Two Wire Serial (TWS) Interface Clock Rate			400	kHz	
Receiver Differential Data Output		100		Ohm	
Link Distance with G.652			10	km	

Electrical Characteristics

Parameter	Min	Typical	Max	Unit	Note
TRx Power Consumption	1.4		2.5	W	
Supply Current			800	mA	

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Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Lane Wavelength	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
Transmitter Optical Characteristics						
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	PT			8.3	dBm	
Average Launch Optical Power, each lane	LOP	-7		2.3	dBm	
Optical Modulation Amplitude, each lane	OMA	-4		3.5	dBm	
Difference in Launch Power between any Two Lanes (OMA)	Ptx,diff			6.5	dB	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TPD), each Lane		-4.8			dBm	
TDP, each lane	TDP			2.6	dB	
Average launch power of OFF transmitter, each lane	Poff			-30	dBm	
Extinction Ratio	ER	3.5			dB	
Relative Intensity Noise	RIN			-128	dB/Hz	
Optical Return Loss Tolerance	TOL			20	dB	
Transmitter Reflectance	R_T			-12	dB	
Receiver Optical Characteristics						
Damage Threshold, each Lane	THd	3.3			dBm	
Average Receive Power, each Lane		-13.7		2.3	dBm	

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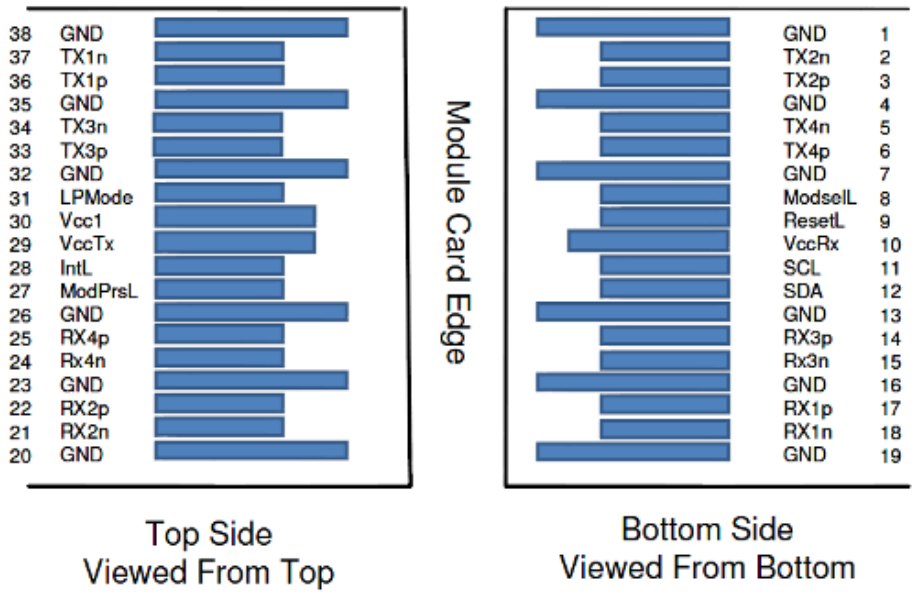
Receive Power (OMA), each Lane				3.5	dBm	
Difference in receive power between any two lanes (OMA)				7.5	dBm	
Receiver reflectance				-26	dB	
Receiver Sensitivity (OMA), each Lane	SEN			-11.5	dBm	
LOS Assert	LosA	-28			dBm	
LOS Deassert	LosD			-15	dBm	
LOS Hysteresis	LosH	0.5		6	dB	

QSFP+ Module Pad Assignments and Descriptions



Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	

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7		GND	Ground	1	
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	
20		GND	Ground	1	
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	
30		Vcc1	+3.3V Power supply	2	
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	

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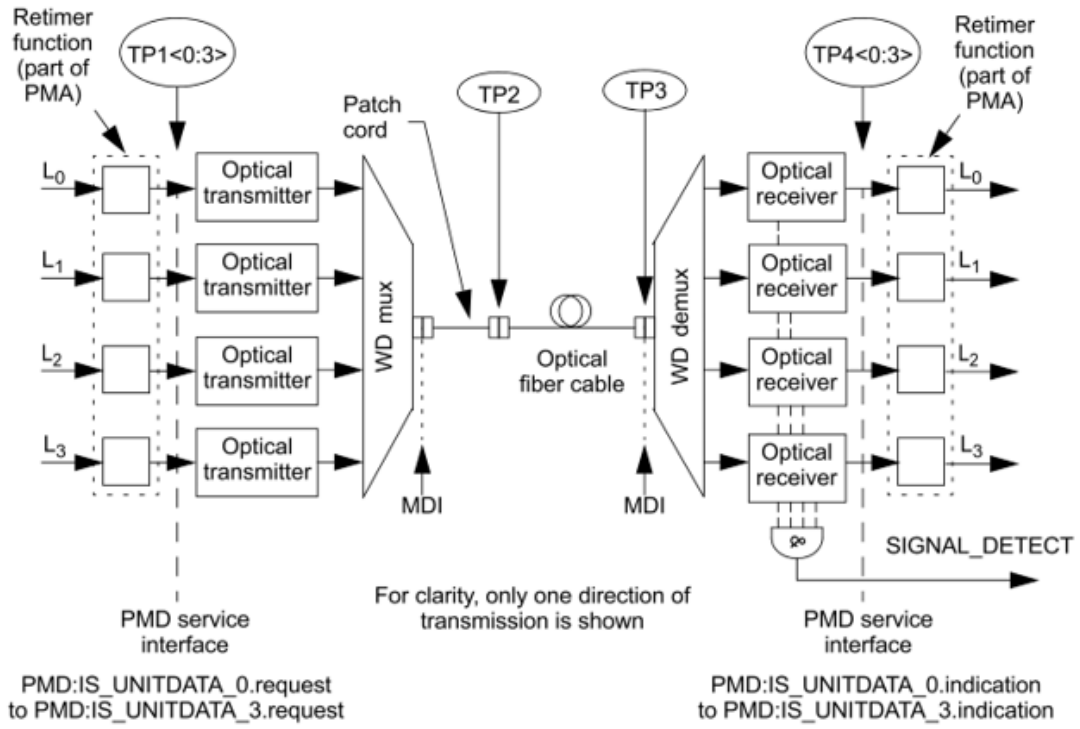
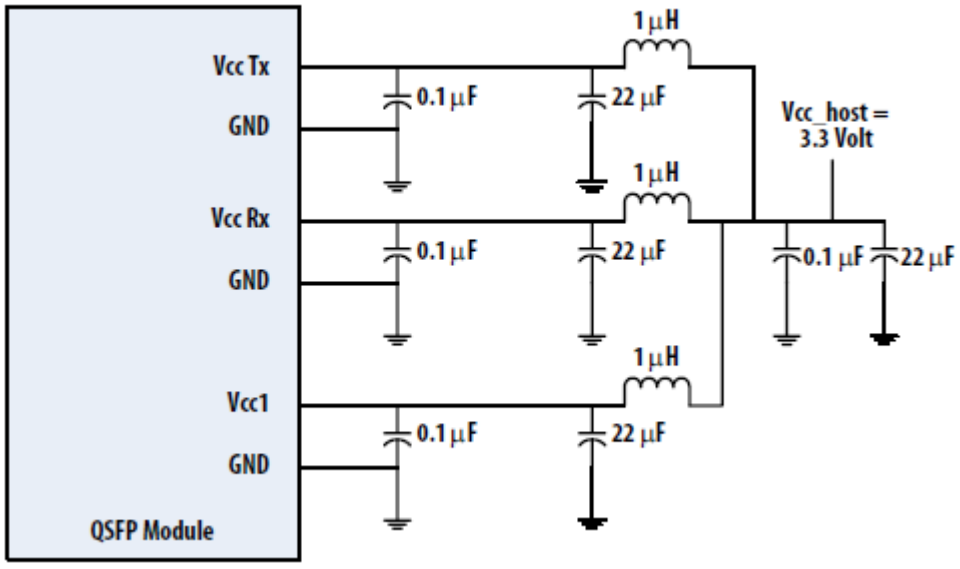
Transceiver Block Diagram

Block diagram for 40GBASE–LR4 transmit/receive paths



NOTE—Specification of the retimer function is beyond the scope of this standard.

Recommended Host Board Power Supply Circuit



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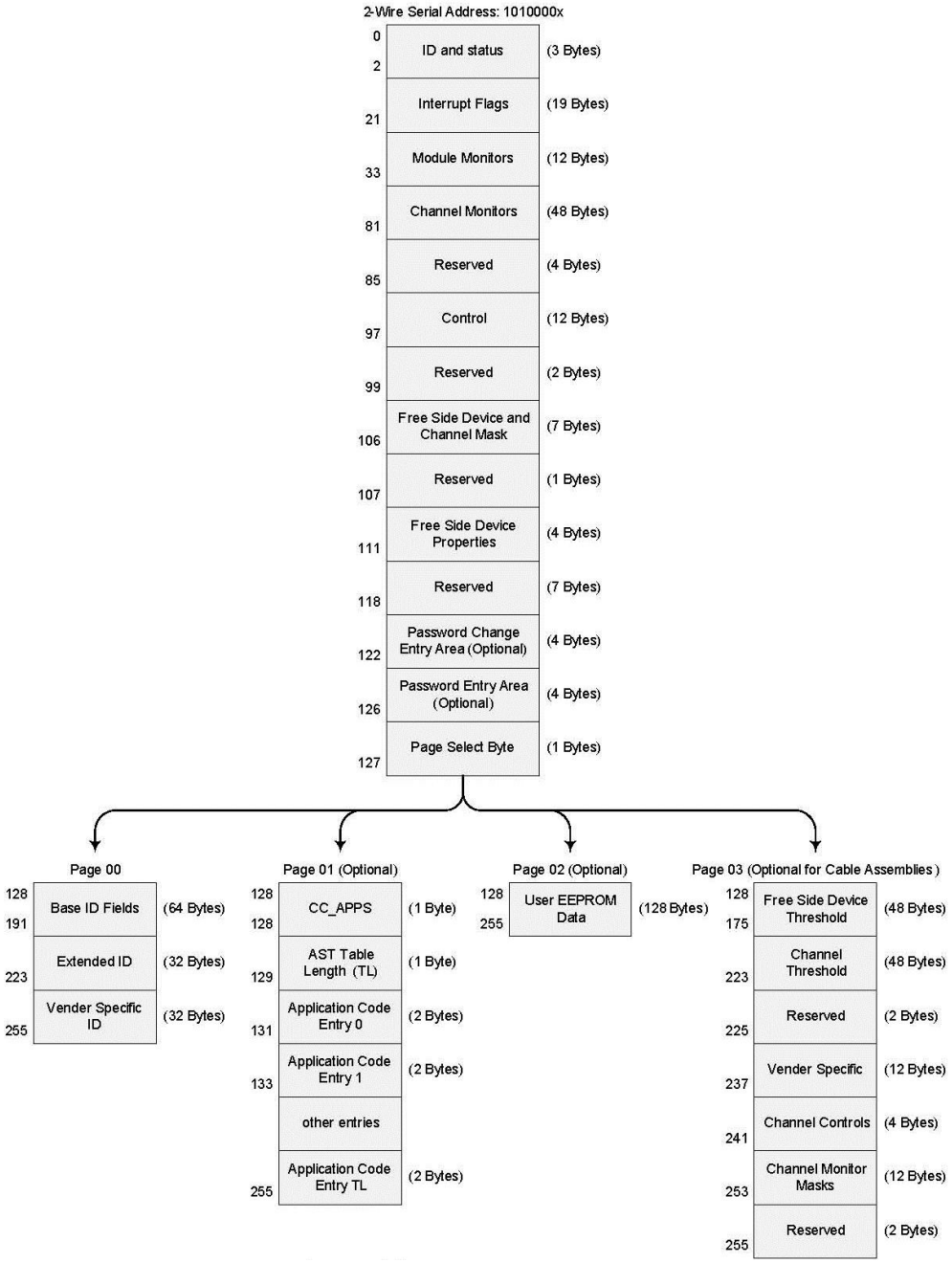
Memory Map

The memory map is structured as a single address and multiple page approaches, according to the QSFP+ SFF-8436 MSA specification as shown in the below. For more detailed description of this memory map or lower pages, please see our Memory Map document with flexible customization settings.



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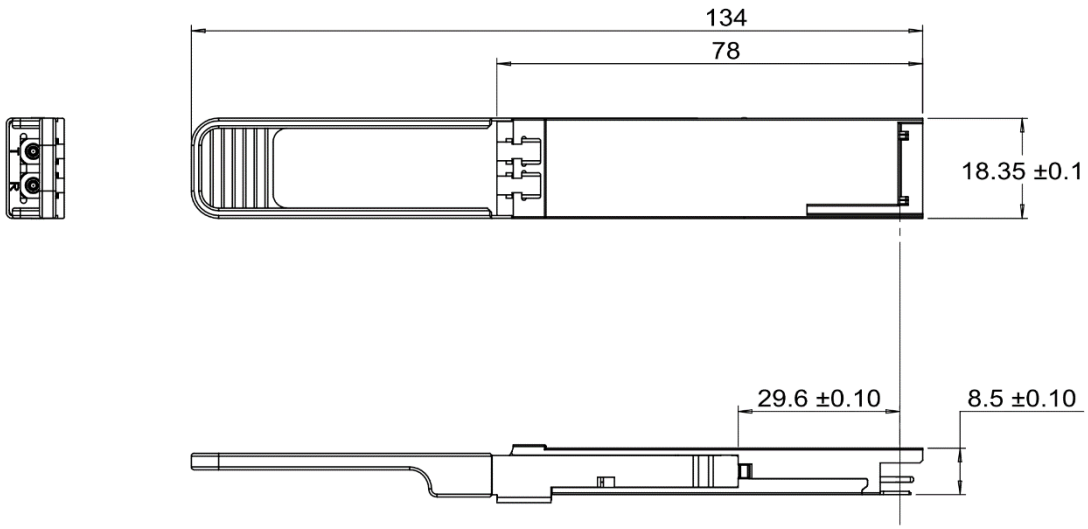
Mechanical Design Diagram

Unit: mm



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