

40Gb/S QSFP+ SR4 Transceiver

P/N: TQSFPP-CJ1A85B



Product Features

- Compliant with IEEE 802.3ba 40G BASE-SR4 standards
- QSFP+ MSA compliant
- Up to 11.2Gbps per channel bandwidth
- Up to 100m OM3 MMF transmission
- TX input and RX output CDR retiming
- Four independent full-duplex channels
- Using standard 12/8 lane optical fiber with MPO pluggable optical connector.
- Single 3.3V power supply
- 0°C to 70°C case temperature operating range
- I2C management interface
- RoHS Compliant

Application

- Ethernet for 40GBASE-SR4
- InfiniBand DDR, SDR, & QDR
- Data Center
- Rack to Rack

Absolute Maximum Rating

Parameter	Min	Max	Unit	Note
Storage Temperature	-40	85	°C	
Power Supply Voltage	-0.5	4	V	
Relative Humidity	0	85	%	

Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Note
Case Operating Temperature	0		70	°C	
Power Supply Voltage	3.135	3.3	3.465	V	
Data Rate per Channel		10.3125		Gbps	
Control Input Voltage High	2		V _{cc}	V	
Control Input Voltage Low	0		0.7	V	
Fiber Length: 50/125µm MMF (OM3)			100	m	
Fiber Length: 50/125µm MMF (OM4)			150	m	

Electrical Characteristics

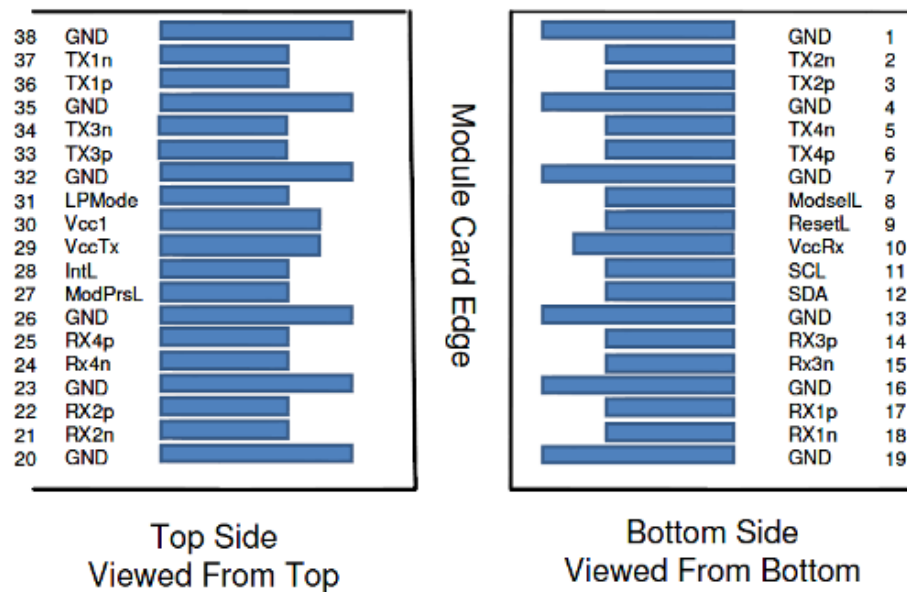
Parameter	Min	Typical	Max	Unit	Note
Transceiver Electrical Characteristics					
TRx Power Consumption			1.5	W	
Supply Current			450	mA	
Transmitter (each Lane)					
Single-ended Input Voltage Tolerance	0.3		4	V	20~80%
AC Common Mode Input Voltage Tolerance	15			mV	
Differential Input Voltage	120		1200	mV	
Differential Input Impedance	80	100	120		
Data Dependent Input Jitter			0.1	UI	
Data Input Total Jitter			0.28	UI	
Receiver (each Lane)					
Single-ended Output Voltage	0.3		4.0	V	
Differential Output Voltage		600	800	mV	

Output Rise and Fall Voltage	Tr/Tf		35	ps	
Total Jitter	TJ		0.7	UI	

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Transmitter Optical Characteristics						
Center Wavelength	λ	840		860	nm	
Spectral Width – RMS	$\Delta\lambda$		0.5	0.65	nm	
Average Launch Optical Power, each lane	LOP	-7.5		0.5	dBm	
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Extinction Ratio	ER	3.0			dB	
Relative Intensity Noise				-128	dB/Hz	12dB reflection
Optical return loss tolerance				12	dB	
Receiver Optical Characteristics						
Center wavelength, each lane	λ	840		860	nm	
Average power at receiver input, each lane		-9.5		2.4	dBm	
Receiver Sensitivity (OMA) per Channel	Sen			-5.4	dBm	
Maximum Input Power		2.4			dBm	
Receiver Reflectance				-12	dB	
LOS De-Assert	LOS _D			-7.5	dBm	
LOS Assert	LOS _A	-20			dBm	
LOS Hysteresis		0.5			dB	

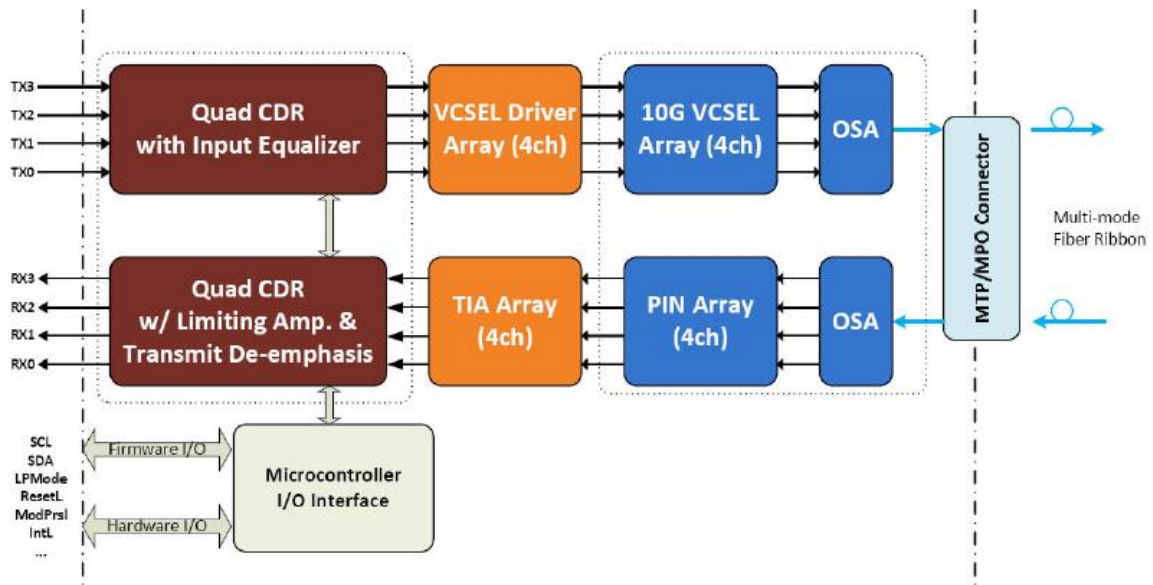
QSFP+ Module Pad Assignments and Descriptions



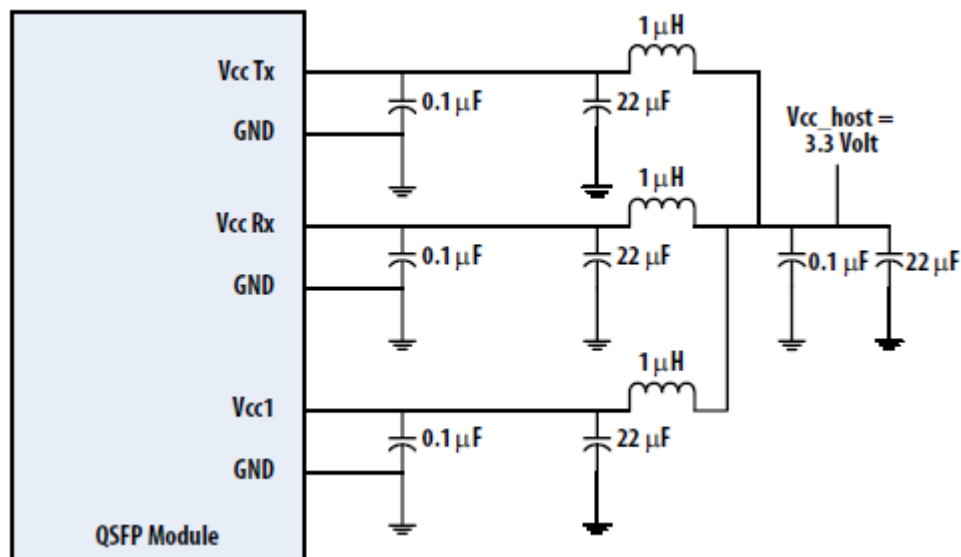
Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	

19		GND	Ground	1	
20		GND	Ground	1	
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	
30		Vcc1	+3.3V Power supply	2	
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	

Transceiver Block Diagram

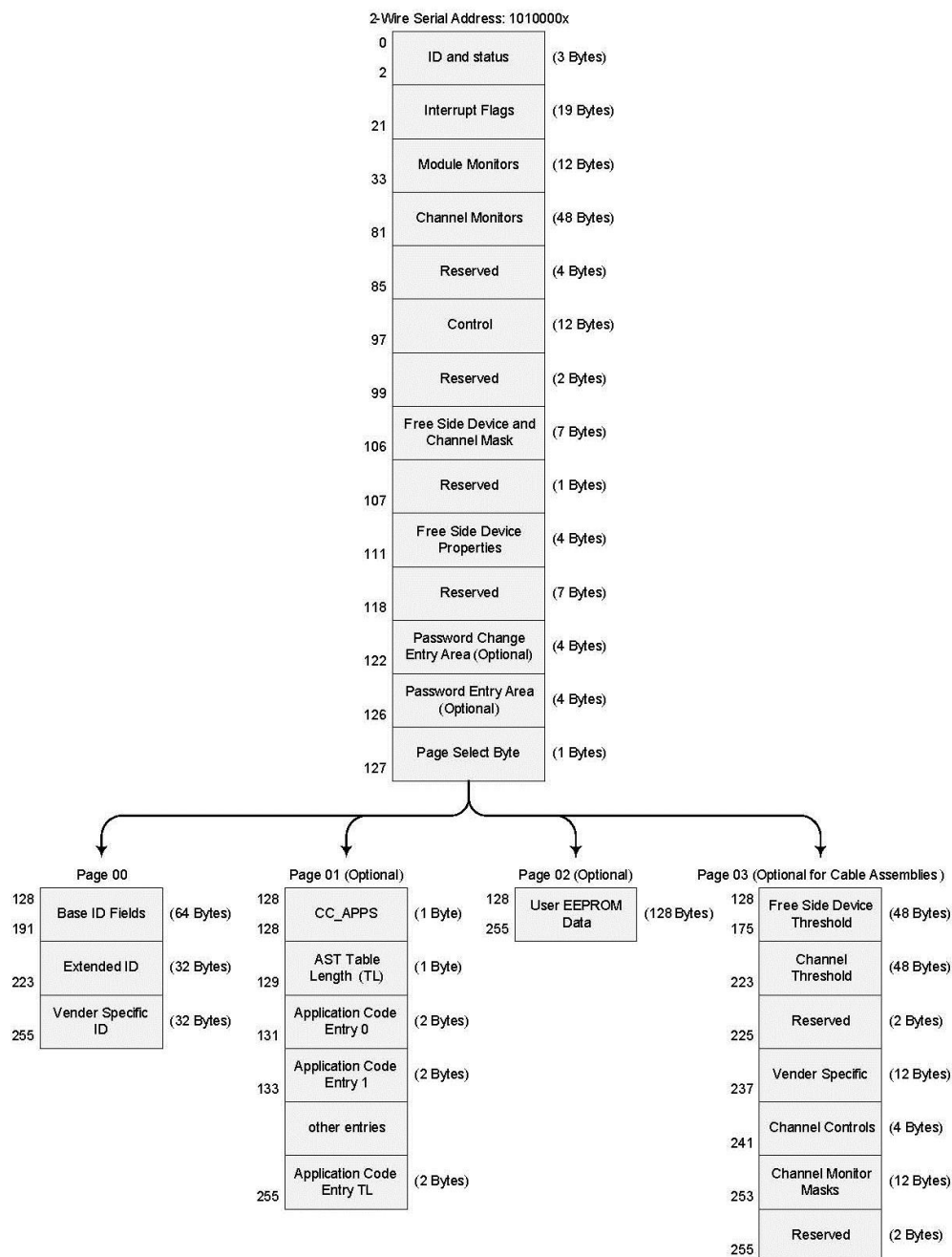


Recommended Host Board Power Supply Circuit



Memory Map

The memory map is structured as a single address and multiple page approaches, according to the QSFP+ SFF-8436 MSA specification as shown in the below. For more detailed description of this memory map or lower pages, please see our Memory Map document with flexible customization settings.



Mechanical Design Diagram

Unit: mm

