100Gb/S QSFP28 LR4 Transceiver

P/N: TQSFP28-EC1FBBA

Product Features

- Compliant with Ethernet IEEE 802.3ba 100G BASE-LR4
- QSFP28 MSA compliant
- Supports 103.1Gb/s aggregate bit rate
- Up to 10km reach for G.652 SMF
- Maximum power consumption 4.0W
- 4x25Gb/s DFB-based LAN-WDM transmitter
- Receiver: 4x25Gb/s PIN ROSA
- Single 3.3V power supply
- 0°C to 70°C case temperature operating range
- 4x25G electrical interface (OIF CEI-28G-VSR)
- Duplex LC receptacle
- I2C management interface
- RoHS-6 Compliant

Application

- 100GBASE-LR4 Ethernet Links
- InfiniBand QDR and DDR interconnects
- Datacenter and Enterprise networking

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Absolute Maximum Rating

Parameter	Min	Max	Unit	Note
Storage Temperature	-40	85	℃	
3.3V Power Supply Voltage	-0.5	3.6	V	
Relative Humidity	0	85	%	
Damage Threshold / Lane	5.5		dBm	

Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Note
Case Operating Temperature	0		70	℃	
Power Supply Voltage	3.135	3.3	3.465	V	
Date Rate per Channel		25.78125		Gbps	
Data Rate Accuracy	-100		100	ppm	
Control Input Voltage High	2		Vcc	V	
Control Input Voltage Low	0		0.8	V	
Link Distance with G.652	0.002		10	km	

Electrical Characteristics

Parameter	Min	Typical	Max	Unit	Note
Transceiver Electrical Characteristics					
TRx Power Consumption			4.0	W	
Supply Current			1.21	A	
Transmitter (each Lane)					
Overload Differential Voltage pk-pk	900			mV	
Common Mode Voltage (Vcm)	-350		2850	mV	1
Differential Termination Resistance Mismatch			10	%	At 1MHz
Differential Return Loss (SDD11)			See CEI-28G-VSR Equation 13-19	dB	
Common Mode to Differential conversion and Differential to			See CEI-28G-VSR	dB	

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Common Mode conversion (SDC11, SCD11)			Equation 13-20		
Stressed Input Test	See CEI-28G-VSR Section 13.3.11.2.1				
Receiver (each Lane)					
Differential Voltage, pk-pk			900	mV	
Common Mode Voltage (Vcm)	-350		2850	mV	1
Common Mode Noise, RMS			17.5	mV	
Differential Termination Resistance Mismatch			10	%	At 1MHz
Differential Return Loss (SDD22)			See CEI-28G-VSR Equation 13-19	dB	
Common Mode to Differential conversion and Differential to Common Mode conversion (SDC22, SCD22)			See CEI-28G-VSR Equation 13-21	dB	
Common Mode Return Loss (SCC22)			-2	dB	2
Transition Time, 20 to 80%	9.5			ps	
Vertical Eye Closure (VEC)			5.5	dB	
Eye Width at 10^{-15} probability (EW15)	0.57			UI	
Eye Height at 10^{-15} probability (EH15)	228			mV	

Notes

1. Vcm is generated by the host. Specification includes effects of ground offset voltage.
2. From 250MHz to 30GHz.

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Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Lane Wavelength	L0	1294.53	1295.56	1296.59	nm	
	L1	1299.02	1300.05	1301.09	nm	
	L2	1303.54	1304.58	1305.63	nm	
	L3	1308.09	1309.14	1310.19	nm	
Transmitter Optical Characteristics						
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	P_T			10.5	dBm	
Average Launch Optical Power, each lane	LOP	-4.3		4.5	dBm	
Optical Modulation Amplitude, each lane	OMA	-1.3		4.5	dBm	1
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane		-2.3			dBm	
TDP, each lane	TDP			2.2	dB	
Average launch power of OFF transmitter, each lane	Poff			-30	dBm	
Extinction Ratio	ER	4			dB	
Difference in Launch Power between any Two Lanes (OMA)	Ptx,diff			5	dB	
$RIN_{20}OMA$	RIN			-130	dB/Hz	
Optical Return Loss Tolerance	TOL			20	dB	
Transmitter Reflectance	R_T			-12	dB	
Eye Mask {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				2
Receiver Optical Characteristics						
Damage Threshold, each Lane	THd	5.5			dBm	3

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Receiver Reflectance				-26	dB	
Average Receive Power, each Lane		-10.6		4.5	dBm	
Receive Power (OMA), each Lane				4.5	dBm	
Receiver Sensitivity (OMA), each Lane	SEN			-8.6	dBm	
Stressed Receiver Sensitivity (OMA), each Lane				-6.8	dBm	4
Difference in Receiver Power between any Two Lanes (OMA)				5.5	dB	
LOS Assert	LosA	-30			dBm	
LOS Deassert	LosD			-13	dBm	
LOS Hysteresis	LosH	0.5			dB	
Receiver Electrical 3dB upper Cutoff Frequency, each Lane	Fc			31	GHz	
Conditions of stressed receiver sensitivity test(Note5):						
Vertical Eye Closure Penalty, each Lane			1.8		dB	
Stressed eye J2 Jitter			0.3		UI	
Stressed eye J9 Jitter,			0.47		UI	

Notes

1. Even if the TDP < 1 dB, the OMA min must exceed the minimum value specified here.
2. Hit ratio $5x10^{-5}$.
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
4. Measured with conformance test signal at receiver input for BER = $1x10^{-12}$

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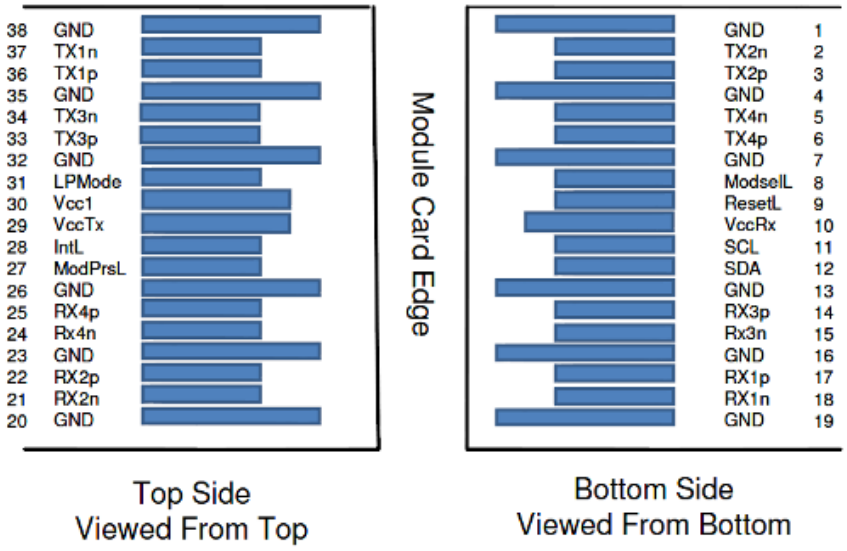
5. Vertical eye closure penalty, stressed eye J2 jitter, and stressed eye J9 jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

QSFP28 Module Pad Assignments and Descriptions



Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	

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14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	
20		GND	Ground	1	
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	
30		Vcc1	+3.3V Power supply	2	
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	

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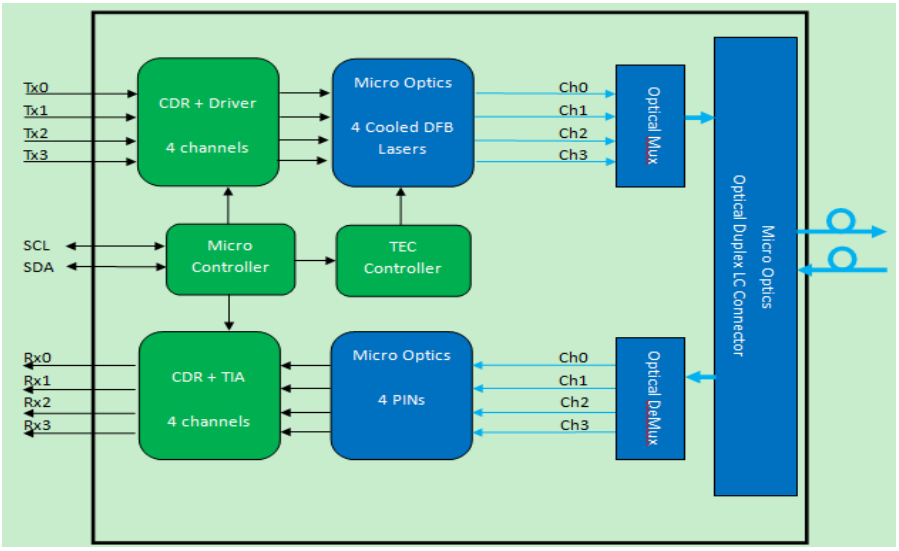
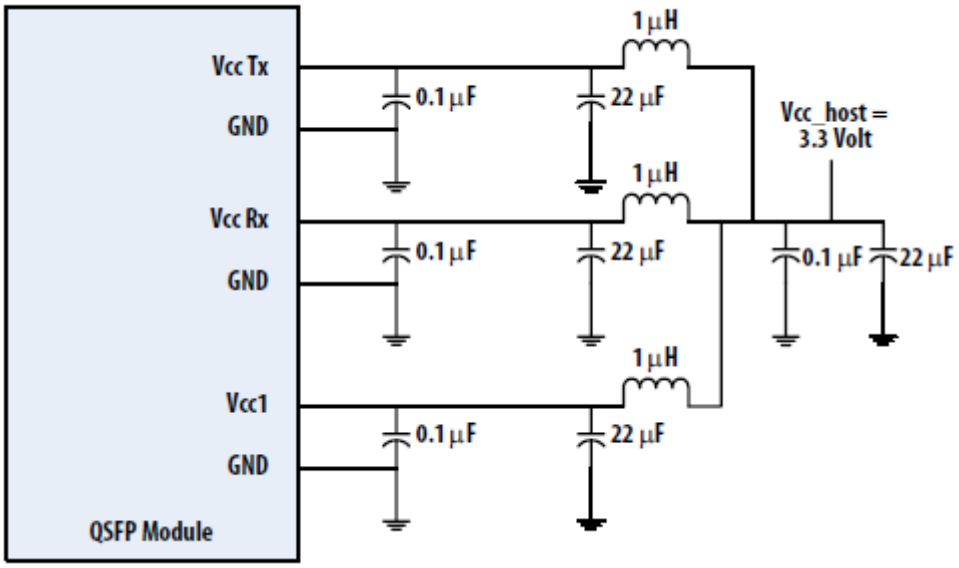
Transceiver Block Diagram



Recommended Host Board Power Supply Circuit



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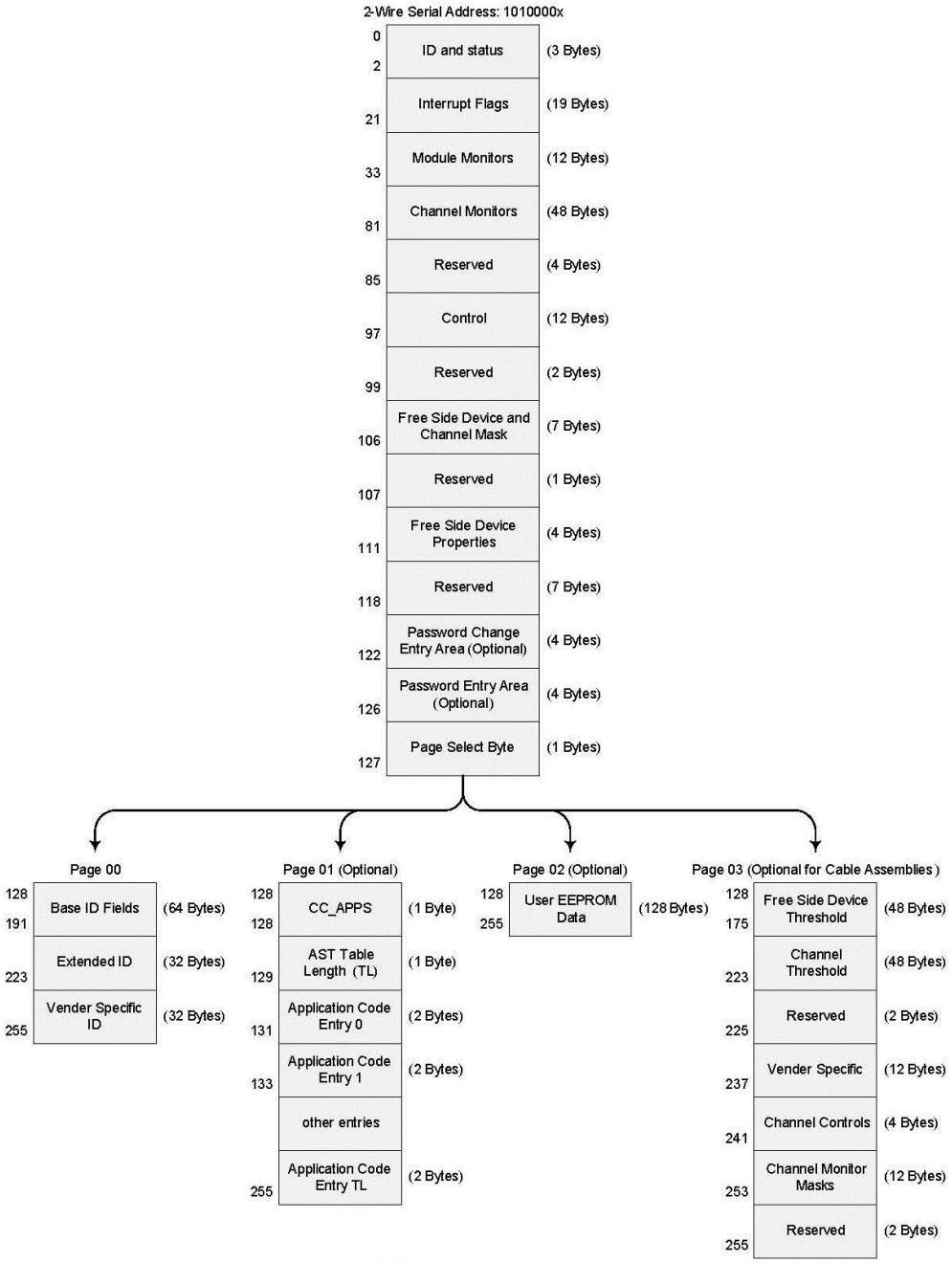
Memory Map

The memory map is structured as a single address and multiple page approaches, according to the QSFP28 SFF-8636 MSA specification as shown in the below. For more detailed description of this memory map or lower pages, please see our Memory Map document with flexible customization settings.



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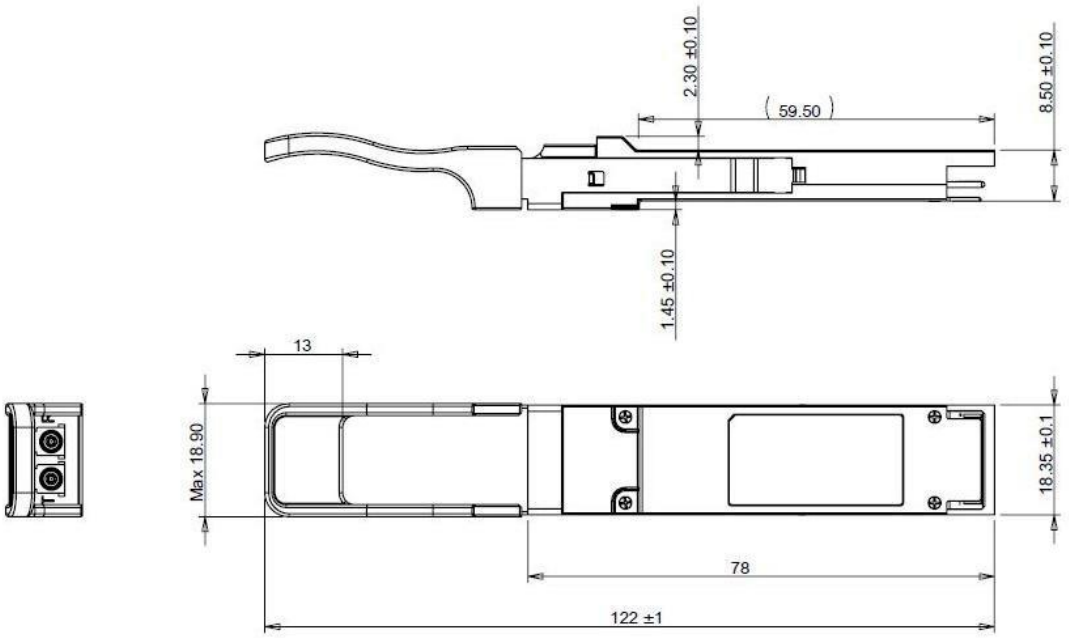
Mechanical Design Diagram

Unit: mm



ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all others electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser Safety

This is a Class 1 Laser Product according to EN 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

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